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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,286	01/22/2004	Toshihiro Terazawa	248034US2	3188

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
CHUNG, PHUNG M	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,286	TERAZAWA, TOSHIHIRO	
	Examiner	Art Unit	
	Phung My Chung	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9,11-16,19 and 20* is/are rejected.

7)☒ Claim(s) *4,10,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sachdev (6,134,688) in view of Whetsel (6,189,115).

As per claim 1, Sachdev discloses a test circuit comprising:

A noninversion/inversion control circuit inserted and connected between a sequential circuit and a combinational circuit, the non-inversion/inversion control circuit not inverting or inverting scan data output from the sequential circuit. (See Figs. 2 and 4) and col. 6, lines 10-30). Sachdev does not disclose that the combinational circuit included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing. However, Whetsel does disclose that the combinational circuit included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing (col. 7, lines 46-67 to col. 9, lines 1-3). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the combinational circuit included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing as taught by Whetsel into the combinational circuit of Sachdev so that testing electrical circuits via serial scan access and to testing techniques which allow circuits to be serially tested in a more efficient manner (col. 1, lines 30-35).

As per claim 2, Whetsel further discloses a multiplexer (MUX) for selecting output according to the control signal.

As per claims 3, 7-9, Sachdev further discloses an inverter to generate inverted data (124).

3. Claims 5-6, 11-16 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sachdev (6,134,688) in view of Whetsel (6,189,115) as applied to claims 1 above, and further in view of the applicant admitted prior art (AAPA).

As per claims 13-14, Sachdev discloses a test circuit comprising:

A first sequential circuit (S1);

A noninversion/inversion control circuit inserted and connected between a sequential circuit and a combinational circuit, the non-inversion/inversion control circuit not inverting or inverting scan data output from the sequential circuit. (See Figs. 2 and 4) and col. 6, lines 10-30). Sachdev does not disclose that the combinational circuit included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing. However, Whetsel does disclose that the combinational circuit included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing (col. 7, lines 46-67 to col. 9, lines 1-3). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the combinational circuit included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing as taught by Whetsel into the combinational circuit of Sachdev so that testing electrical circuits via serial scan access and to testing techniques which allow circuits to be serially tested in a more efficient manner (col. 1,

lines 30-35). Sachdev and Whetsel do not disclose a second sequential circuit to capture output data output from the combinational circuit according to the scan data. However, the AAPA discloses a second sequential circuit (S2) to capture output data output from the combinational circuit (C1) according to the scan data (Fig. 1). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate a second sequential circuit connected to the output of the combinational circuit as taught by the AAPA into the combinational circuit of Sachdev and Whetsel to capture data output from the combinational circuit.

As per claims 5-6, the teaching of Sachdev and Whetsel have been discussed above. They do not disclose that the sequential circuit is a one-phase or two-phase clocked sequential circuit. However, the AAPA discloses that the sequential circuit is a one-phase or two-phase clocked sequential circuit (pg. 1, lines 28-31 and pg. 2, lines 17-20). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the sequential circuit is a one-phase or two-phase clocked sequential circuit as taught by the AAPA into the invention of Sachdev and Whetsel at-speed scan test .

As per claims 11-12 and 19-20, these claim are rejected under similar rationale as set forth in claims 5-6.

As per claim 15, this claim is rejected under similar rationale as set forth in claim 2.

As per claim 16, this claim is rejected under similar rationale as set forth in claim 3.

4. Claims 4, 10 and 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phung My Chung
Primary Patent Examiner
Art Unit 2138

1. The abstract of the disclosure is objected to because it contains the language that can be implied (i.e. "Said").

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sachdev (6,134,688) in view of Whetsel (6,189,115).

As per claim 1, Sachdev discloses a test circuit comprising:

A noninversion/inversion control circuit inserted and connected between a sequential circuit and a combinational circuit, the non-inversion/inversion control circuit not inverting or inverting scan data output from the sequential circuit. (See Figs. 2 and 4) and col. 6, lines 10-30). Sachdev does not disclose that the combinational circuit

included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing. However, Whetsel does disclose that the combinational circuit included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing (col. 7, lines 46-67 to col. 9, lines 1-3). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the combinational circuit included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing as taught by Whetsel into the combinational circuit of Sachdev so that testing electrical circuits via serial scan access and to testing techniques which allow circuits to be serially tested in a more efficient manner (col. 1, lines 30-35).

As per claim 2, Whetsel further discloses a multiplexer (MUX) for selecting output according to the control signal.

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As per claims 13-14, Sachdev discloses a test circuit comprising:

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A noninversion/inversion control circuit inserted and connected between a sequential circuit and a combinational circuit, the non-inversion/inversion control circuit not inverting or inverting scan data output from the sequential circuit. (See Figs. 2 and

4) and col. 6, lines 10-30). Sachdev does not disclose that the combinational circuit included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing. However, Whetsel does disclose that the combinational circuit included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing (col. 7, lines 46-67 to col. 9, lines 1-3). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the combinational circuit included in a path to be subjected to a scan test on outside of the sequential circuit at arbitrary timing as taught by Whetsel into the combinational circuit of Sachdev so that testing electrical circuits via serial scan access and to testing techniques which allow circuits to be serially tested in a more efficient manner (col. 1, lines 30-35). Sachdev and Whetsel do not disclose a second sequential circuit to capture output data output from the combinational circuit according to the scan data. However, the AAPA discloses a second sequential circuit (S2) to capture output data output from the combinational circuit (C1) according to the scan data (Fig. 1). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate a second sequential circuit connected to the output of the combinational circuit as taught by the AAPA into the combinational circuit of Sachdev and Whetsel to capture data output from the combinational circuit.

As per claims 5-6, the teaching of Sachdev and Whetsel have been discussed above. They do not disclose that the sequential circuit is a one-phase or two-phase clocked sequential circuit. However, the AAPA discloses that the sequential circuit is a one-phase or two-phase clocked sequential circuit (pg. 1, lines 28-31 and pg. 2, lines

17-20). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the sequential circuit is a one-phase or two-phase clocked sequential circuit as taught by the AAPA into the invention of Sachdev and Whetsel at-speed scan test .

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Phung My Chung
Primary Patent Examiner
Art Unit 2138